**Lab 6: Introduction to Multiplexers and Decoders**

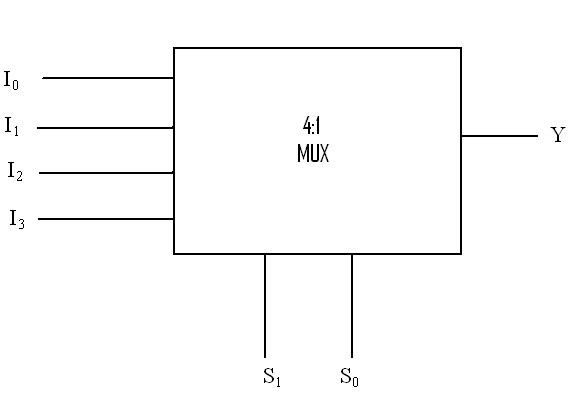
1. **Objectives**

* Understand the concept of multiplexing in the context of digital logic circuits.
* Learn about the internal logic of digital multiplexers.
* Implement digital logic functions using multiplexers.
* Observe and analyze the operations of the 3 to 8 Line Decoder

1. **Theory**

**Multiplexers:** A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2ninput lines and n selection lines whose bit combinations determine which input is selected.

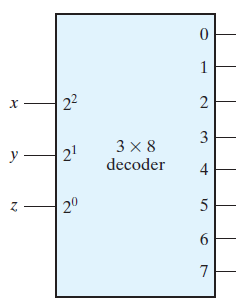
A block diagram and truth table for a 4:1 Multiplexer (4 inputs and 1 output) is given below.



|  |  |  |
| --- | --- | --- |
| **S1** | **S0** | **Y** |
| 0 | 0 | I0 |
| 0 | 1 | I1 |
| 1 | 0 | I2 |
| 1 | 1 | I3 |
| Output Equation:  **Y= I0S1'S0' + I1S1'S2 + I2S1S2' + I3S1S2** | | |

**Table B1:** Truth table for 4:1 Multiplexer

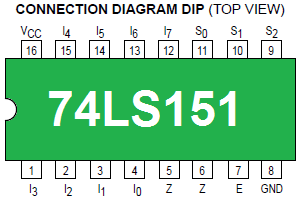
**Figure B1:** Block diagram of 4:1 Multiplexer



**Decoders:** A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n output lines.

**Figure B2** shows the block diagram for a 3 to 8 line decoder. Here, x, y and z are the inputs and the combination of their values determines which output line becomes active. Setting all the input values to zero activates the first output line (0), setting x and y to zero and z to 1 activates the second output line (1) and this pattern continues till all the inputs are 1 at which point the eighth output line (7) is activated.

**Figure B2:** Block diagram of 3 to 8 line decoder



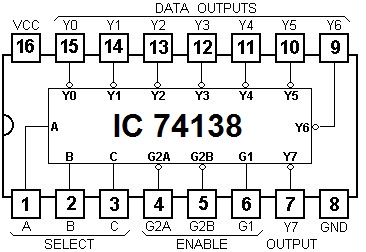
**New Apparatus:**

**IC 74151 (8:1 Multiplexer):**

The 74151 is a 16 pin IC which requires a Ground connection at pin 8 and VCC at pin 16. Pins 4, 3, 2, 1 and 15, 14, 13, 12 are the 8 inputs, pins 9, 10 and 11 are used to select a particular input and pin 5 is the output. Pin 6 is provides the inverse of the output at pin 5. An input at pin 7 is used to Enable the IC.

**Figure B4:** Pinout of IC74151

**IC 74138 (3 to 8 Line Decoder)**:

The 74138 is also a 16 pin IC which requires GND at pin 8 and VCC at pin 16. Pins 15, 14, 13, 12, 11, 10, 9 and 7 are used as the 8 outputs and pins 3, 2 and 1 are used to take input. A combination of the inputs at pins 6, 4 and 5 is used to enable the device. In order for the IC to function as intended, pin 6 (G1) must have a high value and both pins 4 and 5 (G2A and G2B) must have low values.

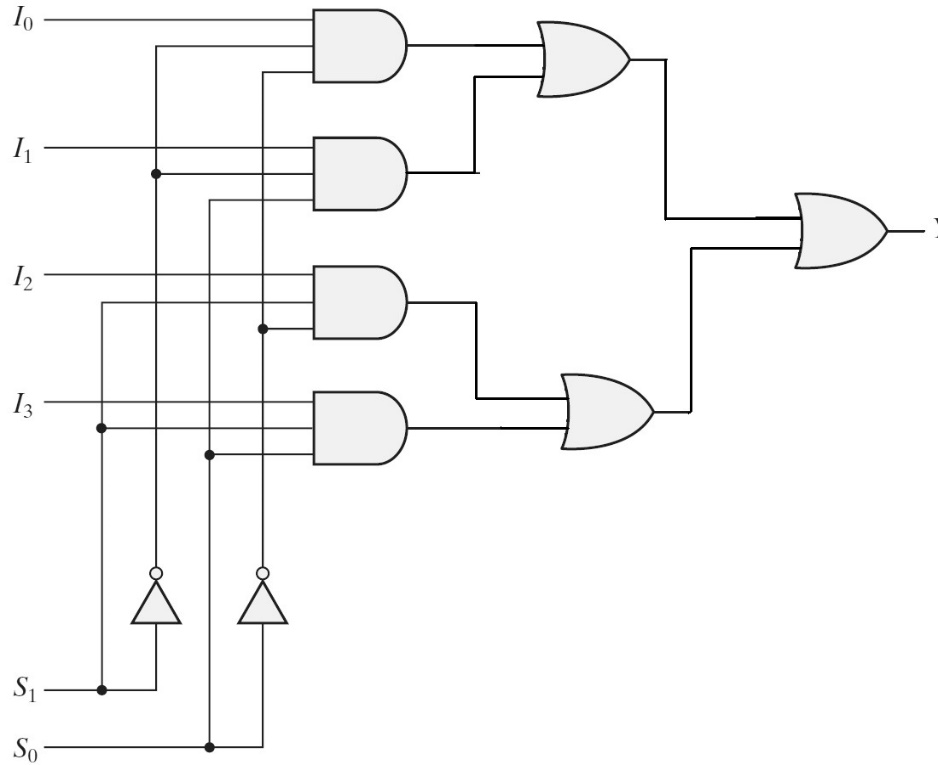
Unlike some of the other ICs used so far, the outputs of the 74138 IC are ACTIVE-LOW which means that they provide a 0 or LOW output when they are activated and a 1 or High output when they are inactive.

**Figure B5:** Pinout of IC74138

**Experiment 1: Constructing a 4:1 Multiplexer using basic Logic Gates**

**C.1 Apparatus**

* Trainer board
* 1 x IC 7404 Hex Inverter (NOT gates)
* 2 x IC 7411 3-input AND gates
* 1 x IC 7432 2-input OR gates

**D.1 Procedure**

**Figure D.1.1** 4:1 Multiplexer

1. Construct the circuit for the 4:1 MUX shown in **Figure D.1.1**.
2. Complete the Theoretical column of the truth table (**Table F.1.1**) for the following function:
   * F(A, B, C) = Σ (0, 1, 5, 7)
3. Now determine the inputs you need to provide to each data input line (I0, I1, I2, I3) of the MUX if you use A and B as the selection inputs, S1 and S0 respectively. Write down the values in the Data Inputs column.
4. Physically implement the function using the 4:1 MUX circuit you constructed.
5. Now complete the Practical column of the truth table.

**E.1 Report**

1. Simulate the circuit with a 4:1 Multiplexer taking B and C as the selection inputs, S1 and S0 respectively using Logisim. Include a screenshot of the circuit with your report.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB Select bit | Io | I1 | I2 | I3 |
| C’ | 1(0) | 0(2) | 0(4) | 0(6) |
| C | 1(1) | 0(3) | 1(5) | 1(7) |
| Input Values | 1 | 0 | C | C |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AC Select bit | Io | I1 | I2 | I3 |
| B’ | 1(0) | 1(1) | 0(4) | 1(5) |
| B | 0(2) | 0(3) | 0(6) | 1(7) |
| Input Values | B’ | B’ | 0 | 1 |

**Experiment 2: Using an 8:1 Multiplexer to implement a Boolean function**

**C.2 Apparatus**

* Trainer board
* 1 x IC 74151 8:1 Multiplexer

**D.2 Procedure**

1. Complete the Theoretical column of the truth table (**Table F.2.1**) for the following function:
   * F(A, B, C, D) = Σ (0, 1, 3, 5, 8, 9, 14, 15)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ABC Select bit | Io | I1 | I2 | I3 | I4 | I5 | I6 | I7 |
| D’ | 1(0) | 0(2) | 0(4) | 0(6) | 1(8) | 0(10) | 0(12) | 1(14) |
| D | 1(1) | 1(3) | 1(5) | 0(7) | 1(9) | 0(11) | 0(13) | 1(15) |
| Input Values | 1 | D | D | 0 | 1 | 0 | 0 | 1 |

1. Now determine the inputs you need to provide to each data input line (I0, I1, I2, I3, I4, I5, I6, I7) of the MUX if you use A, B and C as the selection inputs, S2, S1 and S0 respectively. Write down the values in the Data Inputs column.
2. Draw the IC diagram (**Figure F.2.1**) for the implementation of the function using the provided 8:1 MUX (IC 74151). Clearly label the inputs and outputs that you will use.
3. Implement the function using the 8:1 MUX.
4. Now complete the Practical column of the truth table.

**E.2 Report**

1. Draw the IC diagram (with input values) for the implementation of the following function using IC 74151

Take A, C and D as the selection inputs, S2, S1 and S0 respectively.

* + F(A, B, C, D) = Σ (1, 2, 4, 5, 10, 12, 13)

**Experiment 3: Implementing a 3 to 8 Line Decoder using IC 74138**

**C.3 Apparatus**

* Trainer board
* 1 x IC 74138

**D.3 Procedure**

1. Wire up the IC 74183 using the diagram in **Figure B3** as your reference.
   1. Set the Enable inputs to the appropriate values. G1 should be set to High and both G2A and G2B should be set to Low.
   2. The 3 select inputs (**C B A**) should be connected to 3 binary switches and the 8 outputs should be connected to individual LEDs.
2. Now change the values of the select inputs (**C B A**) to every combination from LLL to HHH and complete the truth table in **Table F.3.1.** In this table, use “**L**” to record a 0 and “**H**” to record a 1.

**E.3 Report**

1. Explain the difference between an active-high and an active-low device.

**F.1 Experimental Data: Implementing a Boolean function using a 4:1 MUX:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **A** | **B** | **C** | **F (Theoretical)** | **Data Inputs** | **F (Practical)** |
| 0 | 0 | 0 | 0 | 1 | I0 = |  |
| 1 | 0 | 0 | 1 | 1 |  |
| 2 | 0 | 1 | 0 | 0 | I1 = |  |
| 3 | 0 | 1 | 1 | 0 |  |
| 4 | 1 | 0 | 0 | 0 | I2 = |  |
| 5 | 1 | 0 | 1 | 1 |  |
| 6 | 1 | 1 | 0 | 0 | I3 = |  |
| 7 | 1 | 1 | 1 | 1 |  |

**Table F.1.1**

**F.2 Experimental Data: Using an 8:1 MUX to implement a Boolean function:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F (Theoretical)** | **Data Inputs** | **F (Practical)** |
| 0 | 0 | 0 | 0 | 1 | I0 = |  |
| 0 | 0 | 0 | 1 | 1 |  |
| 0 | 0 | 1 | 0 | 0 | I1 = |  |
| 0 | 0 | 1 | 1 | 1 |  |
| 0 | 1 | 0 | 0 | 0 | I2 = |  |
| 0 | 1 | 0 | 1 | 1 |  |
| 0 | 1 | 1 | 0 | 0 | I3 = |  |
| 0 | 1 | 1 | 1 | 0 |  |
| 1 | 0 | 0 | 0 | 1 | I4 = |  |
| 1 | 0 | 0 | 1 | 1 |  |
| 1 | 0 | 1 | 0 | 0 | I5 = |  |
| 1 | 0 | 1 | 1 | 0 |  |
| 1 | 1 | 0 | 0 | 0 | I6 = |  |
| 1 | 1 | 0 | 1 | 0 |  |
| 1 | 1 | 1 | 0 | 1 | I7 = |  |
| 1 | 1 | 1 | 1 | 1 |  |

**Table F.2.1**

**Figure F.2.1**

**F.3 Experimental Data: 3 to 8 Line Decoder:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Enable Inputs** | | **Select Inputs** | | | **Outputs** | | | | | | | |
| **G1** | **G2** | **C** | **B** | **A** | **Y0** | **Y1** | **Y2** | **Y3** | **Y4** | **Y5** | **Y6** | **Y7** |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

**Table F.3.1**